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Imparting Asymmetric Source Configuration to Hybridized Multilevel Inverter Topology

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Abstract

The conversion of DC to AC has emerged as a vital technology in present electrical scenario. Voltage source inverters are basically categorized on the basis of output waveform configuration of voltage. The multilevel inverters (MLIs) are considerably emerging with enhanced importance and performance with modern topologies overcoming the shortcomings of classical topologies. In addition to the advantage of reduced component count associated with MLIs, few more performance characteristics (such as fault tolerance capability, charge balance control etc.) play a very key role in the practical implementation of multilevel dc-ac conversion. A structure obtained from hybridization of diode-clamped and T-type topologies is discussed in this paper. The entire mathematical model of the proposed topology is presented. The analysis on the applicability of source-symmetry has been carried out. The performance of the proposed topology has been analyzed through the simulation based results carried out in MATLAB/Simulink.

Key-words: multilevel inverters; classical topologies;T-type inverte; fault tolerance; charge balance control

Introduction

Some applications such as adjustable speed drives, air conditioning, uninterruptible power supplies, induction heating, electric vehicle drives, active filters and renewable energy based electric power generation demands for prominent and efficient DC to AC power conversions [1]- [3]. In this context, multilevel inverters (MLIs) play a very leading role and possess great advantage over the conventional two-level inverters [4]. Some of the merits associated with MLIs are [4]: lesser voltage rating of power switches as compared to the operating voltage, enhanced harmonic profile, reduced filter requirement, lesser d*v*/d*t* stress on the load, lesser electromagnetic interference and so on. Since the introduction of MLIs in 1970s, three topologies have come up with great importance [7]: diode clamped, flying capacitor and cascaded H-bridge converters. Each of the mentioned topologies carries peculiar advantages for specific applications. However, they also have a considerable shortcoming in terms of increase in component count with number of output levels. In this regard, MLIs possess the merit of synthesizing a given voltage level in diversified ways. Such states are called 'redundant states' and these states can be used to obtain control objectives such as fault-tolerant operation, charge balance control, switching frequency distribution [8, 9] etc. Over the past decades, new and novel approach associated with topologies have been reported in the literature with the specific objective of decreasing the component count for higher number of levels so as to get a better quality of output waveform [7]-[13]. However with the reduction in component count, the number of redundant states also decreases considerably leading to the loss of subsequent control flexibility. As a result, many reduced device count topologies can be traced out in which charge balance control cannot be obtained, fault tolerance operation is quite impossible or asymmetric sources cannot be monitored [6]. Therefore, in addition to the

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reduction in component count, preserving one or more of features rendered by redundant states is being actively addressed. Such a topology is proposed by Rao and Sivakumar [14] with three peculiar objectives: (a) improvement of output ac for PV sources as input; (b) fault-tolerance capability in the situations of source/switch failures; and (c) reduction in switching devices as compared to the conventional topologies. In [14], authors have reported the working and validation of five-level inverter with and without fault conditions.

It can be stressed that topology selection is most significantly depend on the application requirements and a thorough study of any particular topology is greatly required to examine its suitability for a given application. However, a very restricted treatment of the topology is presented in [14]. Therefore the objective of this paper is to undertake comprehensive analysis of the proposed topology so that its applicability can be further explored on the basis of associated merits and demerits. Hereafter, the topology in question is referred to as "hybrid topology". The contributions of the paper are summarized below:

- he topology governed by configuration of diode-clamped and T-type is proposed.
- The generalization of the proposed topology is discussed.
- The calculations determining the output voltage and source currents are mentioned.
- The analysis of developing the asymmetric source configuration has been undertaken.

The organization of the paper has been structured in the following manner: In Section II, the hybrid topology is presented with description of diode clamped and T-type legs and principle of synthesis. Section III presents the mathematical calculations and an asymmetric source configuration for the hybrid topology. In section IV, MATLAB/Simulink based simulation results are analyzed to validate the asymmetric source configuration. Conclusion of the proposed work is drawn out and summarized in section V.

Principle of Synthesis

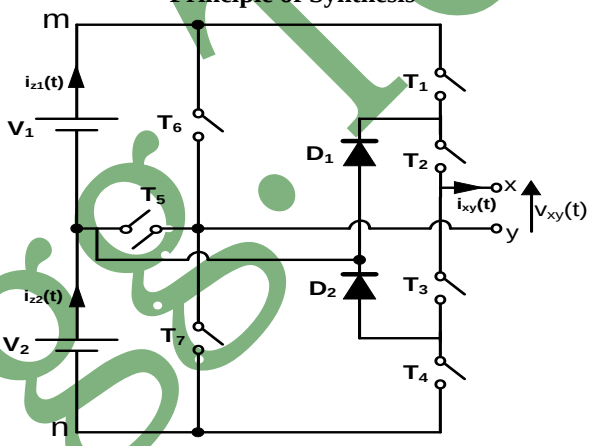
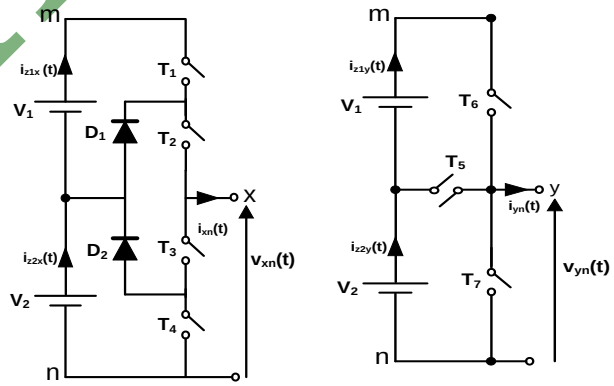


Fig.1. Five-level fault tolerant inverter as proposed in [14]



(a) **(b)**

Fig.2. (a) Diode clamped leg: three-level; (b) T-type leg: three-level

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The configuration proposed under study is five-level topology [14] which is depicted in Fig.1. Authors in [14] have described the hybrid topology to have been synthesized by using a half bridge two-level inverter, three-level diode clamp inverter and a bidirectional switch. As it can be seen in Fig.1, the half bridge two-level inverter is developed by the switches T_6 and T_7. The three-level diode clamped inverter is obtained by the switches T_1, T_2, T_3 and T_4 and clamping diodes D_1 and D_2. Switch T_5 is the bidirectional switch. A deep study of the topology, however, points out that the topology comprises two legs: the right leg is representing a three-level diode clamped structure while the left leg is formed by a three-level T-type structure [15]. In this context, the above-mentioned two legs have been individually being shown in Fig.2. The three-level diode-clamped leg is represented in Fig. 2(a) while the three-level T-type structure is being depicted in Fig. 2(b). Thus, it is quite easy to observe that the topology as depicted in Fig.1 is a hybridization of these topologies, each playing a role as a leg of the hybrid topology. In this reference, it is quite easier to simplify the structure by using the simplified forms of the above topologies being represented by the two legs.

Mathematical Formulations and Asymmetry Considerations

This section describes the involvement of mathematical calculations for the hybrid topology, which are hitherto missed out in [14]. In addition to this, an asymmetric source configuration is also described.

Mathematical Formulations

With the topology in Fig.1, it is quite cumbersome to directly draw a relationship between the key parameters such as output voltage, switching functions and the dc levels of input. It's however simple to determine the relationship especially when the two legs are analyzed individually and the results are combined.

The hybrid topology, as depicted in Fig.1, consists of two rails: positive dc rail '*m*' and negative dc rail '*n*'. $v_{xy}(t)$ *and* $i_{xy}(t)$ respectively represents the output voltage and load current. DC sources V_1 and V_2 supply the respective source currents $i_{z1}(t)$ and $i_{z2}(t)$. In Fig.2(a), the leg representing the three-level diode-clamped portion is depicted with positive and negative dc rails 'm' and '*n*' respectively and dc sources V_1 and V_2 with their respective source currents as $i_{z1x}(t)$ and $i_{z2x}(t)$. To examine the performance, the negative dc rail is taken as the reference. Hence, voltage $v_{xn}(t)$ is represented as output voltage and $i_{xn}(t)$ as the corresponding load current. The values of corresponding voltages and currents for different switching configurations are listed in Table I.

TABLE I. VOLTAGES AND CURRENTS FOR 3-LEVEL DIODE CLAMPED LEG FOR VARIOUS SWITCHING POSITIONS

State	Switches in ON state	Voltage $V_{xn}(t)$	Source current $i_{z1x}(t)$	Source current $i_{z2x}(t)$
1_x	T_1, T_2	$V_1 + V_2$	$i_{xn}(t)$	$i_{xn}(t)$
2_x	T_2, T_3	V_2	0	$i_{xn}(t)$
3_x	T_3, T_4	0	0	0

Accordingly, following expressions can be derived:

$V_{xn}(t) = T_2(1-T_4)\,[T_1V_1 + (T_3 + T_1)V_2]$ (1)

$i_{z1x}(t) = T_1\,T_2\,i_{xn}(t)$ (2)

$i_{z2x}(t) = T_2\,(T_1 + T_3)\,i_{xn}(t)$ (3)

In Fig.2(b), the leg representing the three-level T-type portion is depicted with positive and negative dc rails '*m*' and '*n*' respectively and dc sources V_1 and V_2 with their corresponding source currents as $i_{z1y}(t)$ and $i_{z2y}(t)$. For analyzing the performance, the negative dc rail is considered as the reference. Hence, voltage $v_{yn}(t)$ is depicted as output voltage and $i_{yn}(t)$ as the corresponding load current. The respective values of voltages and currents for different switching positions are listed in Table II.

TABLE II. VOLTAGES AND CURRENTS FOR 3-LEVEL T-TYPE LEG FOR VARIOUS SWITCHING POSITIONS

State	Switch in ON state	Voltage $V_{yn}(t)$	Source current $i_{z1y}(t)$	Source current $i_{z2y}(t)$
1_y	T_5	V_2	0	$i_{yn}(t)$
2_y	T_6	$V_1 + V_2$	$i_{yn}(t)$	$i_{yn}(t)$
3_y	T_7	0	0	0

Accordingly, following expressions are given by:

$v_{yn}(t) = (1-T_7)[T_6\,V_1 + (T_5 + T_6)\,V_2\,]$ (4)

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$i_{z1y}(t) = T_6\, i_{yn}(t)$ (5)
$i_{z2y}(t) = (T_5 + T_6)\, i_{yn}(t)$ (6)
Principle of superposition determines following with the Fig.1 and Fig.2:
$i_{z1}(t) = i_{z1x}(t) + i_{z1y}(t)$ (7)
$i_{z2}(t) = i_{z2x}(t) + i_{z2y}(t)$ (8)
$i_{xn}(t) = i_{xy}(t)$ (9)
$i_{yn}(t) = - i_{xy}(t)$ (10)
$v_{xy}(t) = v_{xn}(t) - v_{yn}(t)$ (11)
With the set of equations (7)-(8) along-with equations (1)-(6), following relations can be derived:
$v_{xy}(t) = \{T_1 T_2(1-T_4) - T_6 (1-T_7)\} V_1$
$+\{T_2(1-T_4)(T_3+T_1)-(1-T_7)(T_5+T_6)\} V_2$ (12)
$i_{z1}(t) = (T_1 T_2 - T_6)\, i_{xy}(t)$ (13)
$i_{z2}(t) = \{T_2 (T_1 + T_3) - (T_5 + T_6)\}\, i_{xy}(t)$ (14)
Equations (12)-(14) governs the mathematical model for the hybrid topology as depicted in Fig.1.

Asymmetry in Source Configuration

The technique proposed in [14] for the hybrid topology is studied by considering the symmetric source configuration, i.e. w.r.t. Fig.1, when $V_1 = V_2$. The popularity of Asymmetric source configurations (i.e the state of unequal source voltages) in multilevel inverters is governed by the reason for decreased power switch count resulting into the rise in number of levels in the output voltage [16]. Thus, in this sub-section, the application of asymmetric sources in the hybrid topology has been analyzed. The type of asymmetry involves the redundant states present in the topology [7]. Different states for the topology shown in Fig.1 are summarized in Table III.

TABLE III. STATES FOR THE TOPOLOGY SHOWN IN FIG.1.

State	Output Voltage $v_{xy}(t)$	State Combination with reference to tables I and II
1	V_1	1_x , 1_y
2	0	1_x , 2_y
3	$V_1 + V_2$	1_x , 3_y
4	0	2_x , 1_y
5	$- V_1$	2_x , 2_y
6	V_2	2_x , 3_y
7	$- V_2$	3_x , 1_y
8	$- V_1 - V_2$	3_x , 2_y
9	0	3_x , 3_y

Table III points out that the topology having total nine states out of which six representing the non-zero voltage states and three as zero-voltage states. In addition, all the non-zero voltage states are unique states. Thus, the proposed topology is suitable enough to synthesize seven unique levels at the output voltage. With considering symmetric source configuration, only five levels are formed. It can be determined that if source voltages are selected in the ratio of 1:2, seven levels can be formed with the same component count as for the five-level structure. Thus with $V_1 = V_{DC}$ and $V_2 = 2V_{DC}$, the voltage levels as obtained will be 0, $\pm V_{DC}$, $\pm 2V_{DC}$ and $\pm 3V_{DC}$, i.e. seven levels in equal step-size of V_{DC}, with states indicated in Table IV.

TABLE IV. STATES FOR THE TOPOLOGY SHOWN IN FIG.1.

State	**Output Voltage $v_{xy}(t)$**	**State Combination with reference to tables I and II**
1	V_{DC}	1_x , 1_y
2	0	1_x , 2_y
3	$3V_{DC}$	1_x , 3_y
4	0	2_x , 1_y
5	$- V_{DC}$	2_x , 2_y
6	$2V_{DC}$	2_x , 3_y
7	$- 2V_{DC}$	3_x , 1_y
8	$-3 V_{DC}$	3_x , 2_y
9	0	3_x , 3_y

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Simulation Results

In order to validate the performance of asymmetric configuration proposed under study, MATLAB/Simulink based model is implemented as shown in Fig.1 with V_1 = 100V and V_2 = 200V. An *RL* load is connected at the load terminals with randomly selected values of R = 5 ohm and L = 6mH. Sinusoidal waveform is considered as the reference and triangular waveforms of frequency 1kHz are utilized as carriers. Arbitrarily selected modulation index of 0.95 is taken. The voltage and current waveforms corresponding to the load are depicted in Fig.3 and Fig.4 respectively. It can be observed that the output voltage is having seven levels with step size of 100 V as desired. Also, the sinusoidal nature of current includes the effect of presence of inductive load. The harmonic nature of load voltage and current are also depicted in Fig.5 and Fig.6 respectively. The obtained results clearly validate performance of the proposed asymmetric source configuration.

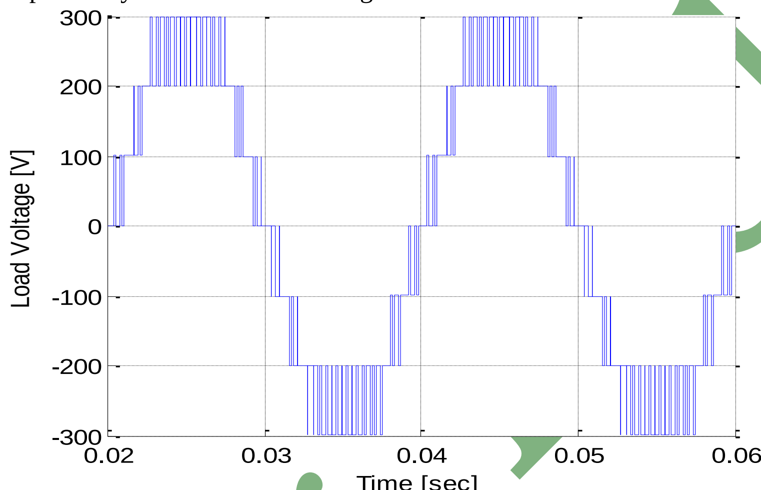

Fig. 3 Output voltage waveform (simulated)

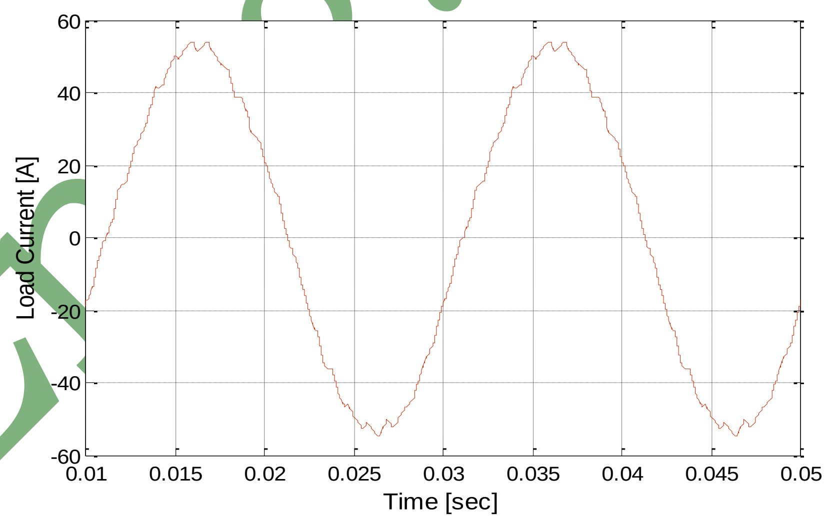

Fig. 4 Output current waveform (simulated)

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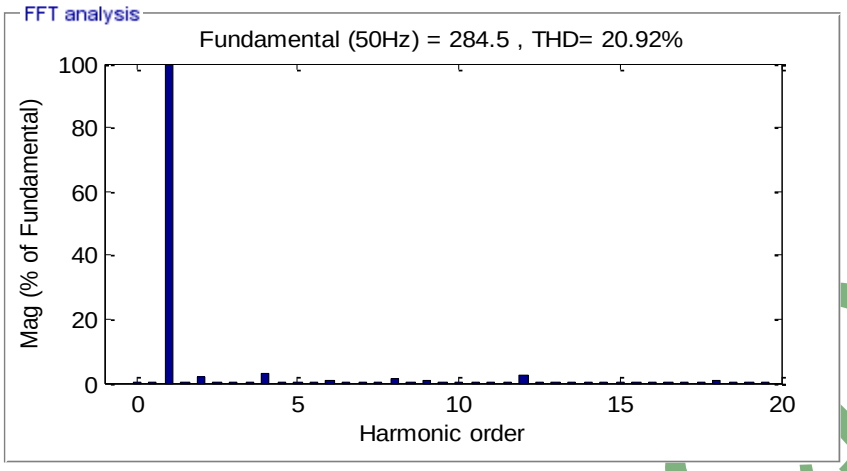

Fig .5 Harmonic profile of output voltage (simulated)

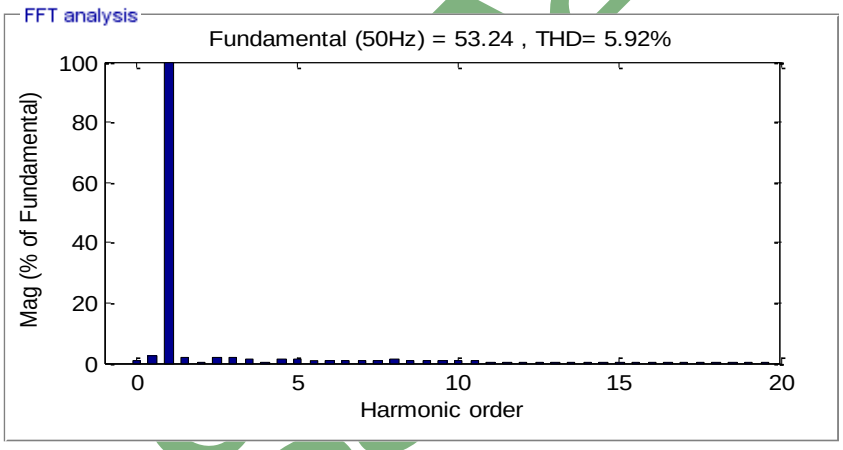

Fig .6 Harmonic profile of output current (simulated)

Conclusion

In this paper a newly proposed topology for multilevel inverter is presented. The principle of synthesis of the hybrid structure is discussed in the paper for comprehensive illustration, generalization and mathematical modeling of the proposed topology. The topology comprises of two legs: a three-level diode clamped inverter and a three-level T-type inverter. Thus, mathematical calculations have been undertaken separately for the legs and then the overall formulations are achieved by consolidating the separate formulations. On the basis of this synthesis, it is observed that the topology can be given asymmetric sources as the input, in this case a binary configuration. In order to analyze the performance of the proposed asymmetry, computer based simulation results are included. Results drawn from the study clearly validates the proposed concepts.

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